3.3.4 Number of research papers per teacher in the Journals notified on UGC website during the last five years (8)

S.No	Academic Year	Count
1	2018-19	9
2	2017-18	6
3	2016-17	6
4	2015-16	3
5	2014-15	0
Total		24

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3.3.4 Number of research papers per teacher in the Journals notified on UGC website during the last five years (8)

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Dr.G.Ramesh,M.E.,Ph.D.,
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Low Power Network-on-Chip Virtual Channel Router Architecture

A.Kalimuthu, Dr.M.Karthikeyan

Department of ECE, JCT college of Engineering and Technology, Principal, Tamilnadu College of Engineering

Kalimuthu.a@jct.ac.in

Abstract— ***Nowadays Network on Chip (NoC) is employed rather than System on Chips (SoCs) for better performance. Because of shrinking technology sizes, more and more processing elements (PEs) and memory blocks are increasingly being integrated on a single chip. But, conventional communication infrastructures can't manage the synchronization issues of the large systems. Using NoCs is a step towards solving that communication problem. For NoC architecture, good performance effective routing algorithms with low power utilization are crucial for real-time applications. In the proposed, we present a novel systematic approach for the router utilizes the concept of acyclic sorting operation which replaces the cyclic round robin arbitration to obtain a low power network on chip router architecture and this architecture is described in detail in this paper. This design achieves reduce the area and decrease in power.***

Keywords—***Network on Chip, router, Bmax unit, Marx unit.***

I. INTRODUCTION

Since the introduction of research into multi-core chips in the late 1990s [1], on-chip networks have emerged as an important and growing field of research. As core counts increase, and multi-core processors emerge in diverse domains ranging from high end servers to Smartphone's and even Internet of Things (IoT) gateways, there is a corresponding increase in bandwidth demand to facilitate high core utilization and a critical need for scalable on-chip interconnection fabrics. This diversity of application platforms has led to research in on-chip networks spanning a variety of disciplines from computer architecture to computer-aided design, embedded systems, VLSI, and more. Here, we provide a synthesis of critical concepts in on-chip networks to quickly bootstrap students and designers into exciting field [2].

In the new computer era, where the design perspective to increase computing performance moves from increasing working frequency of a single core processor system to increasing the number of working processors in a multi-core processor system, the NoC will become a preferred communication infrastructure, when the number of cores will be more than ten cores. A sophisticated communication structure is needed for the inter-processor data exchanges.

NoC came into existence primarily to replace the traditional shared bus networks with wires of shorter lengths which can drastically improve the feasibility and flexibility of the complete system [3]. NoC is basically a packet-based interconnection network, but the flow of data is in flits. Each packet consists of a head flit and body flit where the former has the details of source and destination address and the latter contains the actual data to be transmitted. The significance of NoC [4] is that it can simplify the hardware that controls the routing and switching functions. Routers [5] and Network Interfaces (NIs) form the basic composition of a typical NoC.

The hub of any on-chip network is a router [6] which is categorized functionally into two regimes namely i) Data path and ii) Control Logic. The former constitutes the switch fabric and the latter controls the data flow i.e. the switching [7] of packets from one router to the other or to the NI. The architecture of the router [8] must be kept as simple as possible to reduce area, power and improve speed. This paper presents a new architecture for router which is of less complexity and consumes lower power. Shield is a reliable router architecture which can be tailored with respect to the parameters area, power and delay. The proposed router is a NoC Virtual Channel router consisting of five input and five output ports. Each input port in turn consists of 3 Virtual Channels (buffers). The foundational blocks in the proposed router are Routing Computation Unit, Virtual Channel Allocator Unit, Integrated Switch Allocator and Crossbar Unit and these will be explained in detail in the succeeding section.

Organization of the remaining of the paper is given below. Section II presents a glimpse of Literature Survey referred for this design. Section III describes the complete design of proposed router. Section IV provides the experimental outcomes. Section V concludes this paper.

II. RELATED WORK

Router architecture known for its good reliability [9], [10], [11]. It is more reliable when compared with the baseline router with respect to hard faults. Due to Silicon Protection Factor, it is reliable when evaluated with respect to other router architectures which have the quality of fault tolerance. The results of Shield [11] show that it has 34% and 31% increase in area and power respectively when evaluated with the baseline router. In a nutshell, Shield balances between reliability and the overhead. The switch allocator is used to provide access for flits to the input ports of crossbar and the crossbar is the switch fabric between input

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Performance Analysis of Clustering-Based Topology Generation and disable nodes for NoC

A. Kalimuthu[1*], M. Karthikeyan[2]

[1]Dept. of ECE, JCT College of Engineering and Technology, Coimbatore, India
[2] Tamilnadu College of Engineering, Coimbatore, India

*Corresponding Author: kalimuthu.a@jct.ac.in, Tel.: +91-90420-90231

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Abstract— Network-on-Chips (NoCs) are rapid promising for an on-chip alternative designed in support of many-core System-on-Chips (SoCs). In spite of this, developing an increased overall performance low latency Network on chips using low power overhead has always been a new challenge. Network on Chips (NoCs) by using mesh and torus interconnection topology have become widely used because of the easy construction. A torus structure is nearly the same as the mesh structure, however, has very slighter diameter. The performance of topology can be analyzed based on power and latency; the power consumption and the latency in Network-on-Chip (NoC) are two challenging objectives. In this paper, we proposed on Clustering-Based Topology Generation and disable nodes to construct routers a torus based clustered topology methods for power saving and performances aware on NoC. Experimental results show that the approach saves proposed method consume less power consumption on average in comparison with using torus topology and achieves significant topology performance improvement.

Keywords— NoCs, Cluster, topology generation, disable notes, Routers.

I. INTRODUCTION

Network on Chip (NoC) is realized through the use of Torus structure [1]. They recommended a routing algorithm, router design as well as given solution to the challenge offered from the long wire connection within torus structure through pipe-lining both the long and short wire connection by increase the input buffers connected to the long wires. Because of the fact, gate delays will be scale down along with technology. Large-scale wire delays usually rise tremendously, linearly by including repeaters [3]. The delay may possibly meet or exceed restriction of a clock cycle or repeatedly, a number of clock cycles, in spite of repeater insertion. For ultra deep submicron methods, 75% or a lot of delay with crucial paths may be due to interconnects [4]. Nowadays, Networks on Chip are considered to be a scalable alterative used for on chip communication. Here, the past few decades Network on Chip has appeared like a developing and essential research field.

In Network on Chip, have been proposed to address the several researchers work on topology generation within reasonable time [5],[9],[10], and routing algorithm to improves the performance[8][9]. Mesh and torus are the most commonly used topology. The connection of nodes in the torus is a combination of mesh and regular ring topologies. Torus topology considered as the enlargement of mesh topology. The end nodes in the single column or in the single row are connected to each other directly in torus topology. The number of hop count is reducing in torus compared to mesh topology. The total power in NoC is going to increase with increasing core counts. Therefore, we proposed Clustering-Based Topology Generation using clustering based and disable nodes to construct routers a torus based clustered topology methods for power saving and performances aware. Clustering is dividing the nodes in the network into a different group according to the certain principle. For each group, a node is choosing as a header node which is responsible for the communication between clusters. Internal communication of a cluster is completed within its cluster.

The rest of the paper is organized as follows: section II describes the related work; section III presents methodology our topology generation approach with an example; experimental results are discussed in section IV, and finally the conclusion is made in section V.

II. RELATED WORK

Recently, network-on-chip (NoC) research has focused on the various aspects of on-chip networks, including topology [3], routing algorithms [4, 5], flow control techniques [6], and router architecture [7]. The disable nodes and routers

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ISSN: 1934 – 9955, Volume-10, Issue-4

Deflection Routing Based For NoC Router Architecture Using Pipelining Mechanism

Kalimuthu A, Dr.M.Karthikeyan

Abstract*— Network on Chip (NoC) designers should look at a huge design space. Including creating the right decisions on numerous different design parameters, such as for example topology, routing policy, and flit-width. Additionally, NoC designers should establish the values for each one of these design parameters without violating numerous design limitations, such as real-time delivery, while guaranteeing dead-lock and live-lock avoidance. The resulting NoCs must also provide good performance (e.g. minimal latency and large throughput) at inexpensive (e.g. minimal power and heat dissipation). In this paper, we propose a fault tolerant routing design for NoCs using deflection routing technique within pipeline. That design smartly utilizes fault-free unidirectional links between the routers to forward flits to their destinations in a few number of hops. These links are activating at normal time intervals so they serve as alternate dynamic paths for flits which are tardy because of errors in their computed routes. We also present a routing algorithm that exploits the path diversity in the structure formed by the improved model. From investigational analysis, we obtain substantial development in the network performance parameters like flit- latency, deflection rate and active power dissipation across switch links for the proposed design compared to the state-of-the-art fault tolerant routing techniques in NoC..

***Index Terms*— Network on Chips, Fault-tolerant, Deflection Routing, pipeline .**

I. INTRODUCTION

Network-on-chip (NoC) [4] plays a vital role in message passing and memory access that directly influences the overall performance of multi-core processors. In NoC, the data exchange between cores is realized through the interconnection architecture composed of routers and network interfaces, so when the dark silicon phenomenon occurs, the router connected with the powered-off core still need to keep working to prevent network congestion. Moreover, recent research results show that the power consumption of NoC can be up to 10% -36% [5,6], and most of it comes from routers. Therefore, the optimization design of NoC router becomes important for solving dark silicon problem.

Driven by these observations, in this paper, we carry out the research on the design of low-power NoC router in dark silicon era. The NoC router connected with the powered-off core is only the intermediate node in some routing paths, and is not involved in sending and receiving packets, so it can be powered off. However, the powered-off router has no routing function, and can block packet-forwarding. In order to prevent packet loss, in some studies, when there are some data packets pass through the powered-off router in the network the current router will be woke up frequently by using power-gating technique [8,9,10], which will bring a large network delay and additional power consumption. Therefore, when the injection rate is low, we make the router connected with the powered-off core work in the bypass mode. However, when the network injection rate increases gradually, the router working in the bypass mode may cause network deadlock or too much misrouting. Thus, the router needs to be configured to support routing function. While some studies show that the power consumption of the input buffer accounts for almost half of the router. Therefore, we propose to design a bufferless working mode. In recent years, due to the fact that the bufferless router can greatly reduce the power consumption of NoC, some research have been done in design bufferless router. A proposed bufferless router in [11] uses a simple permutation network instead of the serialized switch allocator and the crossbar to save nearly 48.8% power consumption. However, the router will bring unnecessary deflection of some packets. Therefore, the bufferless working mode we designed is based on deflection times and routing hops, and we propose an input priority judgment method and an output port allocation method to reduce the packet deflection rate. When the injection rate is larger, the packet deflection rate is higher, and the probability of livelock increases gradually, the router working in the designed bufferless mode can be switched to the normal working mode.

Manuscript received October 10, 2018.

A.Kalimuthu, Research Scholar (Ph.D), Computer and Information Technology, Manonmaniam Sundaranar University, Abishekapatti, Tirunelveli 627 012, Tamil Nadu, India.
Mobile No:+91-9042090231, (e-mail:kalimuthu.engg@gamil.com).

Dr.M.Karthikeyan, Principal, Tamilnadu College of Engineering, Coimbatore, India.
Mobile No:+91-9894612700, (e-mail:karthikn_m@hotmail.com)

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Design of D shaped Plasmon – Photonic crystal fiber for Bio Sensing Application

Article *in* Results in Physics · August 2018

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Power Quality Improvement Using DVR Based on DFCM Converter

C.Sakthivel, T.Venkatesan, *K.Selvakumar, C.S Boopathi

Abstract:

In recent years, demand for high power quality and voltage stability has become a pressing issue since power quality issues are perceived as a vital concerns and an oftentimes happening issue having noteworthy exorbitant result, for example, touchy load trip-ping and creation misfortune. Dynamic Voltage Restorer (DVR) is the best and direct answers for "reestablishing" the nature of voltage at its heap side terminals when the nature of voltage at its source-side terminals is aggravated. For medium voltage applications, to connect DVR to medium-voltage power grid, it is needed to use step up line-frequency transformer at the output of DVR. However, this transformer is bulky and heavy and can be a concern in cases with limited area. To avoid this issue, this paper proposes new DVR topol-ogy based on double flying capacitor multicell (DFCM) converter for medium-voltage application. With this ap-proach, there is no need to utilize line-frequency step-up transformer at the output of DVR to match power grid voltage rating. The proposed DVR topology obtains the required active power from the energy storage sustaining the dc connection of the DFCM converter. The fundamental promotion vantages of the proposed converter, in examination with FCM are multiplying the rms and the quantity of yield voltage levels, enhancing the yield voltage recurrence range.The proposed DVR topology is simulated and results to illustrate its performance under various conditions of voltage sag compensation are provided.

Issue: 10-Special Issue

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Hybrid System Using PEMFC

B. Niranjana, J. Priyadharshini, C. Sakthivel and S. Manikandan

Abstract:

In this paper, the distribution grid is connected with a microgrid consisting of different distributed generation (DG) units. The operations of the different DG units in the microgrid for grid-connected and islanded operations are coordinated by the implementation of an energy-management algorithm. The primary generation unit of the microgrid consists of a photovoltaic (PV) array and a proton-exchange membrane fuel cell to supplement the variability in the power generated by the PV array. In the proposed system the Wind energy system in placed in the front end to form a hybrid system. In the back end we have Storage Battery (SB) unit. In order to reduce the fluctuations in the grid and for compensation the system is proposed with the wind system. The design concept is verified through simulating the proposed system using MATLAB Simulink.

Issue: 12-Special Issue

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S. Kanchanadevi[1,b)], S. Parveen[2,c)], *and* V. Mahalingam[3,a)]

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Original Article
First Online: 24 July 2017

Utilization of Auxiliary Winding Power to Improve the Performance of a Single Phase Induction Motor—A Unique Approach

Authors: Jethose, V[1]; Manoharan, S[2]
Source: Journal of Computational and Theoretical Nanoscience, Volume 14, Number 8, August 2017, pp. 3893-3897(5)
Publisher: American Scientific Publishers
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M. Rajasimman [a], S. Venkatesh Babu [b], N. Rajamohan [c]

[a] Department of Chemical Engineering, Annamalai University, Annamalainagar, Tamilnadu 608002, India

Journal of Food Processing and Preservation /
Volume 41, Issue 4

Original Article

Impact of *S. aromaticum* and *C. cassia* Incorporated Edible Films on Shelf Life of Seer Fish (*Scomberomorus guttatus*) Stored at Different Temperature Conditions

Chandra Sekar Chandra Mohan,
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Kasirajan Sudharsan,
Pakirisamy Azhagu Saravana Babu,
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First published: 06 August 2016
https://doi.org/10.1111/jfpp.13096
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Abstract

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Original Article

Polyphenolic and phytochemical content of *Cucumis sativus* seeds and study on mechanism of preservation of nutritional and quality outcomes in enriched mayonnaise

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Summary

Oxidative rancidity in food emulsions leads to a reduction in shelf life

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Volume 68, May 2016, Pages 642-652

Design and characterization of spice fused tamarind starch edible packaging films

C. Chandra mohan [a], K.R. Rakhavan [a], K. Sudharsan [a], K. Radha krishnan [b], S. Babuskin [c], M. Sukumar [a]

[a] Centre for Food Technology, Anna University, Chennai, Tamilnadu, India

[b] Department of Food Processing Technology, CIT, Kokrajhar, Assam, India

[c] JCT College of Engineering & Technology, Coimbatore, Tamilnadu, India

Received 16 July 2015, Revised 3 November 2015, Accepted 4 January 2016, Available onl

LWT - Food Science and Technology

Volume 72, October 2016, Pages 239-250

Development of predictive preservative model for shelf life parameters of beef using response surface methodology

C. Chandra Mohan [a], K.R. Rakhavan [a], K. Radha Krishnan [b], S. Babuskin [c], K. Sudharsan [a], P. Azhagu Saravana Babu [a], M. Sukumar [a]

[a] Centre for Food Technology, Anna University, Chennai, Tamilnadu, India

[b] Department of Food Processing Technology, Central Institute of Technology, Kokrajhar, Assam, India

[c] JCT College of Engineering & Technology, Coimbatore, Tamilnadu, India

Multiple Response Analysis and Optimization of Microwave-Assisted Extraction of Antioxidant Phenolic Compounds of Waste Mangifera indica L Peel

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Carbohydrate Polymers

Volume 123, 5 June 2015, Pages 67-71

Microwave-assisted extraction of pectic polysaccharide from waste mango peel

J. Prakash Maran, K. Swathi, P. Jeevitha, J. Jayalakshmi, G. Ashvini

Department of Food Technology, Kongu Engineering College, Perundurai, Erode 638052, TN, India

Received 19 September 2014, Revised 6 November 2014, Accepted 29 November 2014, Available online 31 December 2014.

J Sci Food Agric. 2016 Sep;96(12):4268-75. doi: 10.1002/jsfa.7638. Epub 2016 Feb 26.

Effect of spice-incorporated starch edible film wrapping on shelf life of white shrimps stored at different temperatures.

Meenatchisundaram S[1], Chandrasekar CM[2], Udayasoorian LP[2], Kavindapadi Rajasekaran R[2], Kesavan RK[3], Srinivasan B[4], Muthusamy S[2].

Author information

Abstract

BACKGROUND: White shrimps (Litopenaeus vannamei) are a major aquaculture product in the world fishery market. The main aim of this study was to investigate the effect of clove- and cinnamon-assimilated starch edible films on the shelf life of white shrimps in terms of maintaining their freshness and other organoleptic properties. Physical, chemical, microbial and sensory qualities of edible film-wrapped white shrimps were studied until they reached their limit of acceptability during storage at different temperatures (10 and 4 °C).

RESULTS: Shrimp samples wrapped with spice-assimilated edible films showed lower bacterial counts. Shelf life extension of edible film-wrapped white shrimps was estimated to be 14 and 12 days for storage at 10 and 4 °C respectively. Reduced lipid oxidation and release of nitrogen base compounds were noted for edible film-wrapped shrimp samples. Good consumer acceptance was noted for edible film-wrapped shrimp samples through sensory evaluation.

CONCLUSION: The results of this study show that spice-fused edible films were effective in inhibiting the growth of microbial populations. Reductions in lipid oxidation and total volatile base nitrogen were also achieved through edible film wrapping of shrimps, which increased their consumer acceptance during sensory evaluation. © 2016 Society of Chemical Industry.

KEYWORDS: edible film; food analysis; food microbiology; shelf life; spices; white shrimps

PMID: 26800104 DOI: 10.1002/jsfa.7638

[Indexed for MEDLINE]

MeSH terms, Substances

MeSH terms

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Food Contamination/analysis
Food Microbiology
Food Packaging/methods*
Food Preservation/methods*
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Microbial Sensitivity Tests
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Penaeidae/chemistry*
Penaeidae/microbiology*
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Seafood/microbiology
Spices*
Starch/chemistry*
Temperature

Substances

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Oils, Volatile